|  |  |  |  |
| --- | --- | --- | --- |
| **Input 1** | **Input 2** | **Sum Output** | **Carry Output** |
| 0 | 0 | **OFF** | **OFF** |
| 0 | 1 | **ON** | **OFF** |
| 1 | 0 | **ON** | **OFF** |
| 1 | 1 | **OFF** | **ON** |

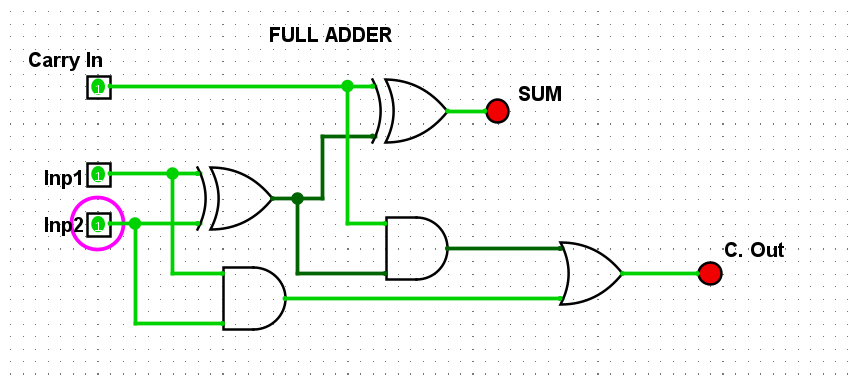
**Half Adder**

Diagram, schematic

Description automatically generated

**Full Adder**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input 1** | **Input 2** | **Carry In** | **Sum Output** | **Carry Output** |
| 0 | 0 | 0 | **OFF** | **ON** |
| 0 | 1 | 0 | **ON** | **OFF** |
| 1 | 0 | 0 | **ON** | **OFF** |
| 1 | 1 | 0 | **OFF** | **ON** |
| 0 | 0 | 1 | **ON** | **OFF** |
| 0 | 1 | 1 | **OFF** | **ON** |
| 1 | 0 | 1 | **OFF** | **ON** |
| 1 | 1 | 1 | **ON** | **ON** |



|  |  |  |
| --- | --- | --- |
| **Input A** | **Input B** | **Output** |
| 0101 | 0000 | **0101** |
| 0101 | 0001 | **0110** |
| 0101 | 0010 | **0111** |
| 0101 | 0011 | **1000** |
| 0101 | 0100 | **1001** |
| 0101 | 0101 | **1010** |
| 0101 | 0110 | **1011** |
| 0101 | 0111 | **1100** |
| 0101 | 1000 | **1101** |
| 0101 | 1001 | **1110** |
| 0101 | 1010 | **1111** |
| 0101 | 1011 | **10000** |
| 0101 | 1100 | **10001** |
| 0101 | 1101 | **10010** |
| 0101 | 1110 | **10011** |
| 0101 | 1111 | **10100** |

Diagram

Description automatically generated